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Field programmable gate array simulation and study on different multiplexer hardware for electronics and communication

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ABSTRACT

Multiplexing is the technique of transmitting two or more separate signals concurrently using a single communication channel. Multiplexing enables the augmentation of communication channels and consequently the volume of data that may be transmitted. Communication networks utilize diverse multiplexing techniques. An input multiplexer amalgamates various network signals into a singular composite signal before transmission over a shared medium. The composite signal is broken back into its component signals by a demultiplexer, when it reaches its destination, allowing further operations to utilize them separately. The design of the hardware chip depends on the configuration of the multiplexer and demultiplexer in the communication system. The work is presented as a study of the digital logic design and simulation of the different configurations of the multiplexer hardware. The performance evaluation is carried out on the different series of Xilinx field programmable gate array (FPGA) such as SPARTAN-6, SPARTAN-3E, Virtex-5, and Virtex-6 with logically checked in Xilinx integrated software environment (ISE) waveform simulator software. The current analysis of the design and simulation of different configurations of the multiplexer design helps the designers to estimate the chip performance. The novelty of the work lies in its scalable and programmable architecture fitted for specific communication systems that assess performance based on latency, frequency, and power consumption that can be further linked with communication protocols.

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1. INTRODUCTION

A multiplexer is a logic circuit that includes several input lines and provides a single output line. It can transmit binary data from one input line to the output line. This is based on the number of inputs corresponding to the selection lines. There are n selection lines and 2n input lines, indicating a multitude of possible input combinations. A multiplexer, commonly known as a Mux or data selector, is a device that selects one data stream from several sources, such as sensors or communication lines, to transmit over the output line. The multiplexer enables the choice of multiple signals coming from multiple sources and communicating to the receiving end based on the desired address of the selection lines to deliver the data to

the receiver. Figure 1 focuses on the signal transition in the analog and digital communication system in which a multiplexer is active on the transmitting end with the source and a demultiplexer on the reception side. Multiplexers and demultiplexers are the most recommended devices employed in both analog and digital communication systems and signal networks. The hardware devices are applied to collective or distinguish many inputs as communication systems that are sent over a particular channel. In an analog communication medium system, the multiplexer signals are combined with several analog signals into a particular signal for transmission. This is beneficial in situations where several signals must be conveyed across a restricted bandwidth channel, such as in cable television or telecommunication systems.

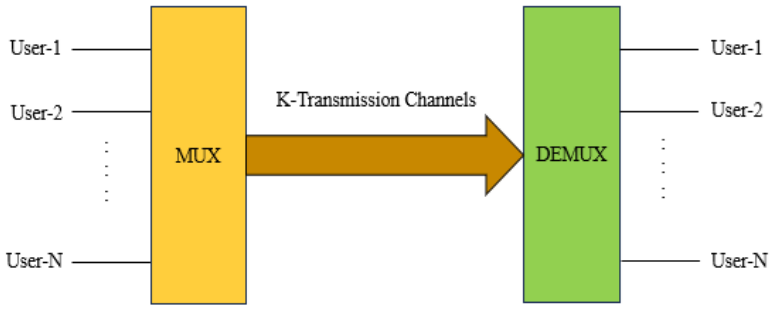


Figure 1. Analog and digital communication system

Different types of switching devices and involved in the transmission system to support the functionality of the multiplexer to decide which signal should be communicated to the receiver. Furthermore, the modulating signal is processed as it is modulated over the carrier wave and communicated over the channel. The different incoming signals are required to segregate and orient them towards the required receiving end. The work is accomplished by the demultiplexer, or demux. Multiplexers and demultiplexers are devices that accomplish comparable functions in digital communication networks, working with digital signals. A digital multiplexer is accountable for cascading numerous digital signals into a single data stream for effective transmission. A demultiplexer is tasked with dividing the distinct signals from the data stream at the receiving end. Digital multiplexers and demultiplexers are frequently active in high-speed data transmission applications. Examples of these applications involve computer networking and digital audio and video systems. These devices can simplify both the accumulation of several data streams into a singular high-speed data link and the disaggregation of individual data streams from such a link. Multiplexers and demultiplexers are decisive elements that enable the effective transmission of several signals over a single channel. These components are utilized in both analog and digital communication systems. The practice of these devices lowers costs and enhances system efficiency by optimizing the essential transmission channels while maintaining the integrity of specific messages. The communication systems [1], [2] consist of various modules, including transmission systems, tributary stations, relay stations, and communication networks. Multiplexing allows the concurrent transmission and parallel data processing with different types of signals and information such as audio and video, over a single communication channel. The modules are employed in telecommunication switching and communication systems consenting several conversations to occur over a single transmission line. Mux can also be used in computers to store more information and use fewer copper wires to connect memory to the various circuit components of a computer. Global positioning system (GPS) satellites in space can also send information to the ground using data signals. Wavelength-division multiplexing (WDM) [3], [4] is a way to send lots of information through a fiber optic cable. It operates by utilizing several colors of light to transmit many signals simultaneously. This indicates that WDM can facilitate swifter and more efficient communication by employing distinct wavelengths (or colors) of light to transmit various signals simultaneously over the same connection. Orthogonal frequency-division multiplexing (OFDM) [5], [6] is a way to send lots of information through the air or over cables. It works by breaking up the data into smaller pieces and sending them over many different narrowband signals called subcarriers [7]. OFDM transmits data at comparable velocities while consuming reduced power. Spatial multiplexing, commonly referred to as space-division multiplexing (SDM), is a method for transmitting numerous independent data channels simultaneously through air or cables [8]. It operates by employing several antennas or fibers to convey signals in various directions or via distinct pathways [9]. This approach is employed in MIMO wireless communication, fiber-optic communication, and various other communication technologies to enhance the volume of data transferred concurrently. Mode-division multiplexing (MDM) technology enables the transmission of substantial data volumes between locations via

cable or fiber optic lines [10]. It achieves this by utilizing many light modes, enabling the simultaneous transmission of multiple signals. In comparison to alternative methods, this suggests that MDM facilitates communication that is both swifter and more efficient. MDM can be applied across diverse systems and applications, from object evaluation using light to sophisticated technologies like quantum optics. The reseparation of multiplexed signals into their original streams is essential for precise decoding and transmission to their designated destinations. Demultiplexing directs each signal to the appropriate receiver or application. Demultiplexing reinstates data integrity by reverting data streams to their original format, therefore preventing any data loss. It ensures accurate stream identification and allocation to the specified user or process. Despite utilizing the same channel, demultiplexing enables multiple processes to independently manage distinct data streams. This guarantees efficient processing. The problem statement of the work is to understand the hardware complexity of the different sizes of multiplexers.

2. RELATED WORK

The multiplexer is used for E and W band applications [11] of multilayer liquid crystal polymer (LCP) substrate as a frequency divider with a directional filter. The multiplexer is a device used in optical communication and a plasmonic [12] multiplexer is a basic element in optical integrated circuits. The multiplexer has practical uses in the creation of photonic [13] integrated systems, the development of optical signal processors, and the establishment of optical networking. An optical add/drop [14] multiplexer is a device that helps protect transmission links in an optical access network, which is growing fast. It provides high-speed, secure, and long-range communication. A multiplexer latch is an important part that helps enable high-speed communication [15] measured in Gbps through a serializer interface. One commonly used method for boosting data transmission rates in visible light communication (VLC) fiber systems is to employ WDM [16]. New methods have been created to see through things that scatter light, like fog or tissue. These methods use something called speckle multiplexing [17] and they are being used in many different areas. Radio frequency-based WDM [18] for free space optical communication by using M-ary pulse position modulation (M-ary PPM) and analysis of the impact of pointing error (PE), amplified spontaneous emission noise, and inter-channel crosstalk. OFDM [19] and differential phase shift key (DPSK) for inter-satellite wireless link. This work includes the transmission of 10 Gbps of data over 20,000 Km using inter satellite optical wireless link (OWL). This was followed by radio frequency optical communication in free space based on spatial mode multiplexing (SMM) [20], multiple input multiple outputs (MIMO), and orbital angular momentum (OAM) in the condition of atmospheric turbulence. The photonic lantern is used as a mode multiplexer [21] in multimode optical telecommunications applications by using SDM. However, the high capacity under [22] water optical communication is based on SDM by using OAM. This work also includes digital signal processing (DSP) algorithm to alleviate the inter-mode crosstalk caused by the temperature variations.

In addition to so, tissue systems biology in health care applications is also based on multiplexed [23] imaging. This work also includes clinical pathology, quantitative pathology, single-cell analysis, imaging mass cytometry, and multiplexed ion beam imaging. Following this an orthogonal frequency-division multiplexing access (OFDMA) technique used for VLC [24] minimizes the possible switching delay and hence supports audio and video signals in real time. Therefore, a bidirectional hybrid OFDM is used in wireless-over-fiber [25] architecture at the optical line terminal (OLT) by utilizing the polarization multiplexing technique. The polarization modulation and polarization multiplexing [26] are used to make a coupled frequency-doubling optoelectronic oscillator (OEO) which can generate a 9.95 GHz signal for fundamental microwave and 19.9 GHz for frequency-doubled microwave. A multichannel and compact hybrid-multiplexed [27] potentiated is designed for conducting electrochemical measurements at continuously-biased electrode arrays. A photonic circuit path is a setup by employing time division multiplexed [28] distributed arbitration in a photonic mesh network. The multiplexed H.264/AVC videoconference sources [29] are used to create a discrete autoregressive model to explore the statistics of busty video signals. Multiplexers [20] are an important instrument for the transmission of signals in optical communication by using optoelectronics devices.

Moreover, in Fiber optic communications, spatial multiplexing [30] facilitates numerous channels within an optical Fiber by assigning a distinct spatial location to each channel, thereby utilizing optical energy effectively. An optical add/drop multiplexer is utilized in the construction of a chaotic signal-generating and cancelation system for nonlinear optical communication [31]. Optical code division multiplexing (OCDM) is utilized in multi-terabit-per-second optoelectronic networks [32]. A frequency-selective [33] multiplexer is designed for microwave switching by combining single-dimensional photonic band gap (PBG) structures. Multiplexed particle-based flow cytometric assays [34] simultaneously measure many various analytes in a small sample volume of tissue culture and biological fluids samples, like

bioassays, enzyme-linked immunosorbent assay (ELISA), recombinase polymerase amplification (RPA), and polymerase chain reaction (PCR). The design of multiplexing and demultiplexing hardware must work well to handle large amounts of data sent over networks like phone lines, computer networks, and satellite communications, and to make communication systems more efficient while cutting costs [35], [36]. The architecture of a multiplexer may differ based on factors such as the number of inputs, the number of select lines, and the logic for input selection [37], [38].

3. DESIGN APPROACH

The design of the different configurations is followed based on the different sizes such as (2×1), (4×1), (8×1), (16×1), (32×1), and (64×1). The behavior of the design is understood based on the function table, logic diagram, and governing equations. The selection inputs play a very important role in the multiplexer design. For a configurable multiplexer (2^n ×1), the 'n' presents the selection inputs.

3.1. (2×1) Mux

A 2×1 multiplexer is a simple device that has two input options, I_0 and I_1, and one selection line, S_0. It has only one output, Y, which is connected to either I_0 or I_1 depending on the signal received by S_0. The (2×1) multiplexer's block representation, functional table, logical equation, and a logical diagram are provided below for reference. Figure 2 presents the block representation of (2×1) Mux, and its logic level representation is presented in Figure 3. The logical expression for (2×1) Mux is given in (1). Table 1 presents the functionality of (2×1) Mux.

$$Y = \bar{S}_0 I_0 + S_0 I_1 \quad (1)$$

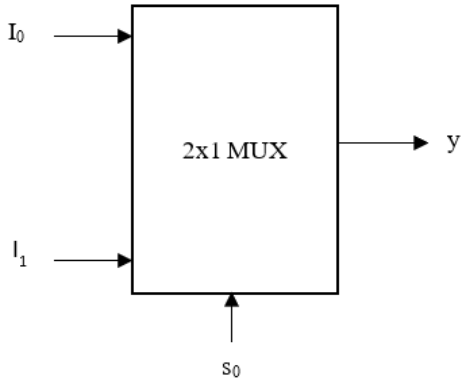


Figure 2. Block representation of (2×1) Mux

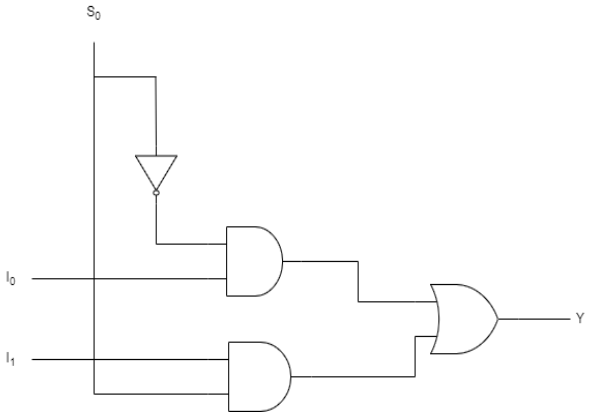


Figure 3. Logical diagram of (2×1) Mux

Table 1. Functional table of (2×1) Mux

Input	Output
S_0	Y
0	I_0
1	I_1

3.2. (4×1) Mux

A (4×1) multiplexer has four input options: I_0, I_1, I_2, and I_3, along with two selection lines, S_0 and S_1. It has one output, Y, which is connected to one of the four inputs based on the signals received by S_0 and S_1. The 4×1 multiplexer's block representation, functional table, logical equation, and logical diagram are provided below for reference. Figure 4 presents the block representation of (2×1) Mux, and its logic level representation is presented in Figure 5. The logical expression for (4×1) Mux is given in (2). Table 2 presents the functionality of (4×1) Mux.

$$Y = \bar{S}_0 \bar{S}_1 I_0 + \bar{S}_0 S I_1 + S_0 \bar{S}_1 I_2 + S_0 S_1 I_3 \quad (2)$$

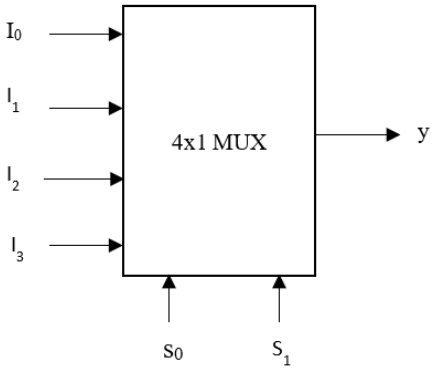


Figure 4. Block representation of (4×1) Mux

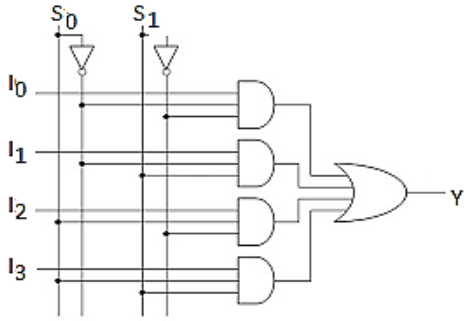


Figure 5. Logical diagram of (4×1) Mux

Table 2. Functional table of (4×1) Mux

Input		Output
S_0	S_1	Y
0	0	0
0	1	0
1	0	1
1	1	1

3.3. (64×1) Mux

The (64×1) multiplexer is a device that has a total of 64 input options, from I_0 to I_{64}, and six selection lines, S_0 to S_5. It has one output, Y, which is connected to one of the 64 inputs depending on the signals received by S_0 to S_5. The functional Table 3 for the (64×1) multiplexer is given below to help understand the output selection based on the combination of input signals received by the selection lines.

Table 3. Functional table of (64×1) Mux

Inputs						Outputs
S_0	S_1	S_2	S_3	S_4	S_5	Y
0	0	0	0	0	0	I_0
0	0	0	0	0	1	I_1
0	0	0	0	1	0	I_2
0	0	0	0	1	1	I_3
0	0	0	1	0	0	I_4
0	0	0	1	0	1	I_5
0	0	0	1	1	0	I_6
0	0	0	1	1	1	I_7
0	0	1	0	0	0	I_8
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	0	I_{62}
1	1	1	1	1	1	I_{63}

The logical expressions of the output of (8×1), (16×1), (32×1), and (64×1) are given by (3) to (6) respectively. The (8×1) Mux: in the logical form, the output Y is given in (3); the (16×1) Mux: in the logical form, output Y is given in (4); the (32×1) Mux: in the logical form the output Y is given in (5); the (64×1) Mux: on the logical form the output Y is given in (6). Similarly, the block representations of (8×1), (16×1), (32×1), and (64×1) are given in Figures 6 to 9 respectively.

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2 I_0 +_0 \bar{S}_1 S_2 I_1 + \bar{S}_0 S_1 \bar{S}_2 I_2 + \bar{S}_0 S_1 S_2 I_3 + S_0\bar{S}_1\bar{S}_2 I_4 + S_0\bar{S}_1 S_2 I_5 + S_0 S_1\bar{S}_2 I_6 + S_0 S_1 S_2 I_7 \quad (3)$$

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2\,\bar{S}_3 I_0 + \bar{S}_0\bar{S}_1\bar{S}_2\,S_3 I_1 + \bar{S}_0\,\bar{S}_1 S_2\bar{S}_3 I_2 + \bar{S}_0\bar{S}_1 S_2 S_3 I_3 + \bar{S}_0 S_1\bar{S}_2\bar{S}_3 I_4 + \bar{S}_0 S_1\bar{S}_2 S_3 I_5 + \bar{S}_0 S_1 S_2\bar{S}_3 I_6 + \bar{S}_0 S_1 S_2 S_3 I_7 + S_0\bar{S}_1\bar{S}_2\,\bar{S}_3 I_8 + S_0\bar{S}_1\bar{S}_2 S_3 I_9 + S_0\bar{S}_1 S_2\bar{S}_3 I_{10} + S_0\bar{S}_1 S_2 S_3 I_{11} + S_0 S_1\bar{S}_2\bar{S}_3\, I_{12} + S_0 S_1\bar{S}_2 S_3 I_{13} + S_0 S_1 S_2\bar{S}_3 I_{14} + S_0 S_1 S_2 S_3 I_{15} \quad (4)$$

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4I_0 + \bar{S}_0\bar{S}_1\bar{S}_2\bar{S}_3S_4I_1 + \bar{S}_0\bar{S}_1\bar{S}_2S_3\bar{S}_4I_2 + \bar{S}_0\,\bar{S}_1\bar{S}_2S_3S_4I_3 + \bar{S}_0\bar{S}_1S_2\bar{S}_3\bar{S}_4I_4 + \bar{S}_0\bar{S}_1S_2\bar{S}_3S_4I_5 + \bar{S}_0\bar{S}_1S_2S_3\bar{S}_4I_6 + \bar{S}_0\bar{S}_1S_2S_3S_4I_7 + \bar{S}_0S_1\bar{S}_2\bar{S}_3\bar{S}_4I_8 + \bar{S}_0S_1\bar{S}_2\bar{S}_3S_4I_9 + \bar{S}_0S_1\bar{S}_2S_3\bar{S}_4I_{10} + \bar{S}_0S_1\bar{S}_2\,S_3S_4I_{11} + \bar{S}_0S_1S_2\bar{S}_3\bar{S}_4I_{12} + \bar{S}_0S_1S_2\bar{S}_3S_4I_{13} + \bar{S}_0S_1S_2S_3\bar{S}_4I_{14} + \bar{S}_0S_1S_2S_3S_4I_{15} + S_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4I_{16} + S_0\bar{S}_1\bar{S}_2\bar{S}_3S_4I_{17} + S_0\bar{S}_1\bar{S}_2S_3\bar{S}_4I_{18} + S_0\bar{S}_1\bar{S}_2S_3S_4I_{19} + S_0\bar{S}_1S_2\bar{S}_3\bar{S}_4I_{20} + S_0\bar{S}_1S_2\bar{S}_3S_4I_{21} + S_0\bar{S}_1S_2S_3\bar{S}_4I_{22} + S_0\bar{S}_1S_2S_3S_4I_{23} + S_0S_1\bar{S}_2\bar{S}_3\bar{S}_4I_{24} + S_0S_1\bar{S}_2\bar{S}_3S_4I_{25} + S_0S_1\bar{S}_2S_3\bar{S}_4I_{26} + S_0S_1\bar{S}_2\,S_3S_4I_{27} + S_0S_1S_2\bar{S}_3\bar{S}_4I_{28} + S_0S_1S_2\bar{S}_3S_4I_{29} + S_0S_1S_2S_3\bar{S}_4I_{30} + S_0S_1S_2S_3S_4I_{31} \quad (5)$$

$$Y = \bar{S}_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4\bar{S}_5I_0 + \bar{S}_0\bar{S}_1\bar{S}_2\bar{S}_3\bar{S}_4S_5I_1 + \bar{S}_0\bar{S}_1\bar{S}_2\bar{S}_3S_4\bar{S}_5I_2 + \bar{S}_0\,\bar{S}_1\bar{S}_2\bar{S}_3S_4S_5I_3 + \bar{S}_0\bar{S}_1\bar{S}_2S_3\bar{S}_4\bar{S}_5I_4 + \bar{S}_0\bar{S}_1\bar{S}_2S_3S_4\bar{S}_5I_5 + \bar{S}_0\bar{S}_1\bar{S}_2S_3S_4S_5I_6 + \bar{S}_0\bar{S}_1S_2\bar{S}_3\bar{S}_4\bar{S}_5I_7 + \bar{S}_0\bar{S}_1S_2\bar{S}_3\bar{S}_4S_5I_8 + \bar{S}_0\bar{S}_1S_2\bar{S}_3S_4\bar{S}_5I_9 + \bar{S}_0\bar{S}_1S_2\bar{S}_3S_4S_5I_{10} + \bar{S}_0\bar{S}_1S_2S_3\bar{S}_4\bar{S}_5I_{11} + \bar{S}_0\bar{S}_1S_2S_3\bar{S}_4S_5I_{12} + \bar{S}_0\bar{S}_1S_2S_3S_4\bar{S}_5I_{13} + \bar{S}_0\bar{S}_1S_2S_3S_4S_5I_{14} + \bar{S}_0S_1\bar{S}_2\bar{S}_3\,\bar{S}_4\bar{S}_5I_{15} + \bar{S}_0S_1\bar{S}_2\bar{S}_3\bar{S}_4S_5I_{16} + \bar{S}_0S_1\bar{S}_2\bar{S}_3S_4\bar{S}_5I_{17} + \bar{S}_0S_1\bar{S}_2\bar{S}_3S_4S_5I_{18} + \bar{S}_0S_1\bar{S}_2S_3\bar{S}_4\bar{S}_5I_{19} + \bar{S}_0S_1\bar{S}_2S_3\bar{S}_4S_5I_{20} + \bar{S}_0S_1\bar{S}_2S_3S_4\bar{S}_5I_{21} + \bar{S}_0S_1\bar{S}_2S_3S_4S_5I_{22} + \bar{S}_0S_1S_2\bar{S}_3\bar{S}_4\bar{S}_5I_{23} + \bar{S}_0S_1S_2\bar{S}_3\bar{S}_4S_5I_{24} + \bar{S}_0S_1S_2\bar{S}_3S_4\bar{S}_5I_{25} + \bar{S}_0S_1S_2S_3\bar{S}_4\bar{S}_5I_{26} + \bar{S}_0S_1S_2S_3\,S_4S_5I_{27} + \bar{S}_0S_1S_2S_3S_4\bar{S}_5I_{28} + \bar{S}_0S_1S_2S_3S_4S_5I_{29} + \bar{S}_0S_1S_2S_3S_4\bar{S}_5I_{30} + \bar{S}_0S_1S_2S_3S_4S_5I_{31} + S_0\bar{S}_1\bar{S}_2\,\bar{S}_3\bar{S}_4\bar{S}_5I_{32} + S_0\bar{S}_1\bar{S}_2\bar{S}_3\bar{S}_4S_5I_{33} + S_0\bar{S}_1\bar{S}_2\bar{S}_3S_4\bar{S}_5I_{34} + S_0\bar{S}_1\bar{S}_2\bar{S}_3S_4S_5I_{35} + S_0\bar{S}_1\bar{S}_2S_3\bar{S}_4\bar{S}_5I_{36} + S_0\bar{S}_1\bar{S}_2S_3\bar{S}_4S_5I_{37} + S_0\bar{S}_1\bar{S}_2S_3S_4\bar{S}_5I_{38} + S_0\bar{S}_1\bar{S}_2S_3S_4S_5I_{39} + S_0\bar{S}_1S_2\bar{S}_3\bar{S}_4\bar{S}_5I_{40} + S_0\bar{S}_1S_2\bar{S}_3\bar{S}_4S_5I_{41} + S_0\bar{S}_1S_2\bar{S}_3S_4\bar{S}_5I_{42} + S_0\bar{S}_1S_2\bar{S}_3\,S_4S_5I_{43} + S_0\bar{S}_1S_2S_3\bar{S}_4\bar{S}_5I_{44} + S_0\bar{S}_1S_2S_3\bar{S}_4S_5I_{45} + S_0\bar{S}_1S_2S_3S_4\bar{S}_5I_{46} + S_0\bar{S}_1S_2S_3S_4S_5I_{47} + S_0S_1\bar{S}_2\bar{S}_3\,\bar{S}_4\bar{S}_5I_{48} + S_0S_1\bar{S}_2\bar{S}_3\bar{S}_4S_5I_{49} + S_0S_1\bar{S}_2\bar{S}_3S_4\bar{S}_5I_{50} + S_0S_1\bar{S}_2\bar{S}_3S_4S_5I_{51} + S_0S_1\bar{S}_2S_3\bar{S}_4\bar{S}_5I_{52} + S_0S_1\bar{S}_2S_3\bar{S}_4S_5I_{53} + S_0S_1\bar{S}_2S_3S_4\bar{S}_5I_{54} + S_0S_1\bar{S}_2S_3S_4S_5I_{55} + S_0S_1S_2\bar{S}_3\bar{S}_4\bar{S}_5I_{56} + S_0S_1S_2\bar{S}_3\bar{S}_4S_5I_{57} + S_0S_1S_2\bar{S}_3S_4\bar{S}_5I_{58} + S_0\,S_1S_2\bar{S}_3\,S_4S_5I_{59} + S_0\,S_1S_2S_3\bar{S}_4\bar{S}_5I_{60} + S_0S_1S_2S_3\bar{S}_4S_5I_{61} + S_0S_1S_2S_3S_4\bar{S}_5I_{62} + S_0S_1S_2S_3S_4S_5I_{63} \quad (6)$$

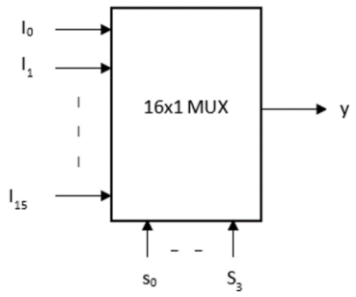


Figure 6. Block representation of (8×1) Mux

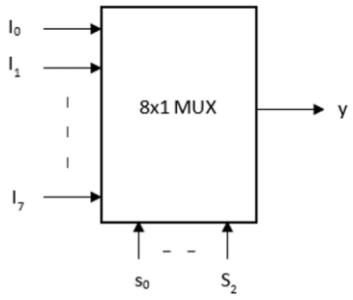


Figure 7. Block representation of (16×1) Mux

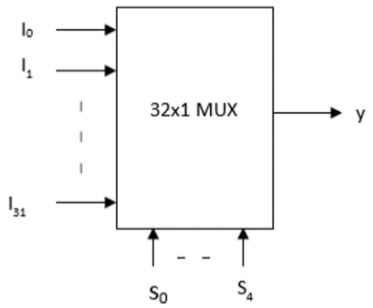


Figure 8. Block representation of (32×1) Mux

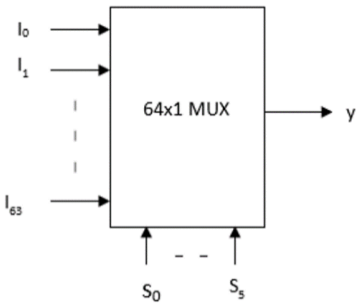
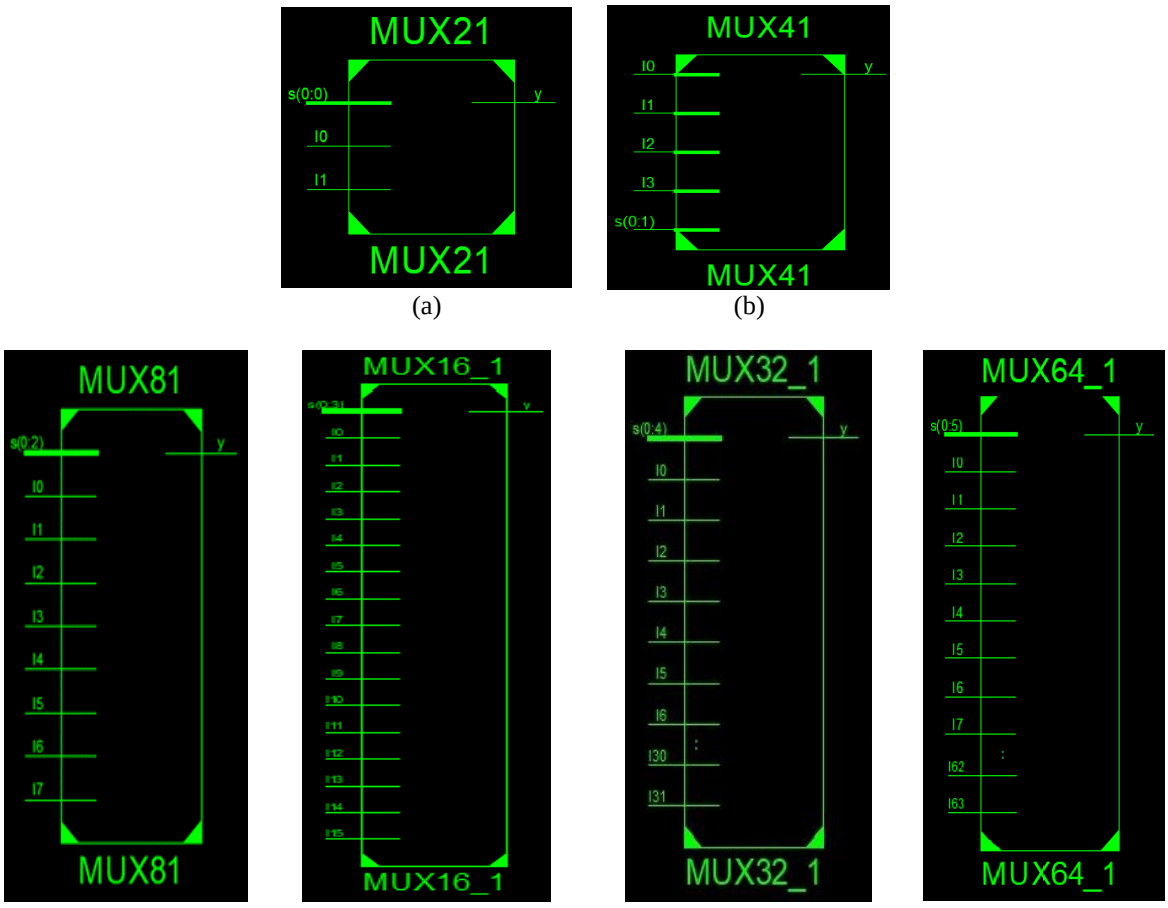


Figure 9. Block representation of (64×1**)** Mux

4. RESULTS AND DISCUSSION

The simulation of (2×1), (4×1), (8×1), (16×1), (32×1), and (64×1) Mux are carried out in Xilinx ISE14.7. The register transfer level (RTL) description in Figure 10 and the result obtained are shown in Figures 10(a) to 10(f). The RTL lists the input and output of the design. Table 4 lists the description of the pins utilized in the design. Very high speed integrated circuit hardware description language (VHDL) code delineates the transformation of data during register transfers in RTL. The data transformation transpires due to the combinational logic positioned between the registers.



(a) (b) (c) (d) (e) (f)

Figure 10. RTL view of (a) (2×1); (b) (4×1); (c) (8×1); (d) (16×1); (e) (32×1), and (f) (64×1) Mux

Table 4. RTL description based on pins

Pins	Description
I_0 <input><1-bit>	Presents the (0^{th}) input pin of the multiplexer (64×1)
I_1 <input><1-bit>	Presents the (1^{st}) input pin of the multiplexer (64×1)
I_2 <input><1-bit>	Presents the (2^{nd}) input pin of the multiplexer (64×1)
I_3 <input><1-bit>	Presents the (3^{rd}) input pin of the multiplexer (64×1)
:	:
I_{63} <input><1-bit>	Presents the (63^{rd}) input pin of the multiplexer (64×1)
S_0 <input><1-bit>	Presents the (0^{th}) position selection input pin of the multiplexer (64×1)
S_1 <input><1-bit>	Presents the (1^{st}) position selection input pin of the multiplexer (64×1)
S_2 <input><1-bit>	Presents the (2^{nd}) position selection input pin of the multiplexer (64×1)
S_3 <input><1-bit>	Presents the (3^{rd}) position selection input pin of the multiplexer (64×1)
S_4 <input><1-bit>	Presents the (4^{th}) position selection input pin of the multiplexer (64×1)
S_5 <input><1-bit>	Presents the (5^{th}) position selection input pin of the multiplexer (64×1)
Y<Output><1-bit>	Presents the output pin of the multiplexer (64×1)

Figures 11 to 16 show the simulation results taken from the integrated simulator (ISIM) simulation in Xilinx for different sizes of multiplexer (2×1), (4×1), (8×1), (16×1), (32×1), and (64×1) respectively. The simulation verification relies on the inputs designated I_0 to I_{63}, based on the selection logic inputs S_0 to S_5, which determine the output. The multiplexer exhibits high efficiency in directing many input signals to a single output signal according to control signals.

Table 5 shows the results obtained from various field programmable gate array (FPGA) such as Virtex-5, Virtex–6, SPARTAN-3E, and SPARTAN-6. From the table, it is observed that the performance of FPGAs in terms of the number of slices, look-up tables (LUTs), and delays is improving with higher configurations. These parameters are extracted directly from the software by choosing the different FPGA and device configurations. The hardware parameters are increasing as the size of the multiplexer configuration is increasing.

The results compare the performance of different multiplexers across four different FPGA families: Virtex-5, SPARTAN-3E, Virtex-6, and SPARTAN-6. The data provides insights into resource usage, delay, memory consumption, and power consumption for each configuration. The Virtex-5 family exhibits a relatively high-power consumption for the 64×1 Mux, with a delay of 5.871 ns. The SPARTAN-3E configuration has a higher delay (9.138 ns) compared to the Virtex-5, and a slightly higher power consumption of 625.00 mW. The Virtex-6 Mux provides the lowest delay of 2.440 ns among all configurations, along with a relatively lower power consumption of 550.30 mW, making it the most efficient in terms of performance. The SPARTAN-6 Mux shows a delay of 8.003 ns and a power consumption of 618.00 mW, placing it between the SPARTAN-3E and Virtex-5 configurations in terms of performance.

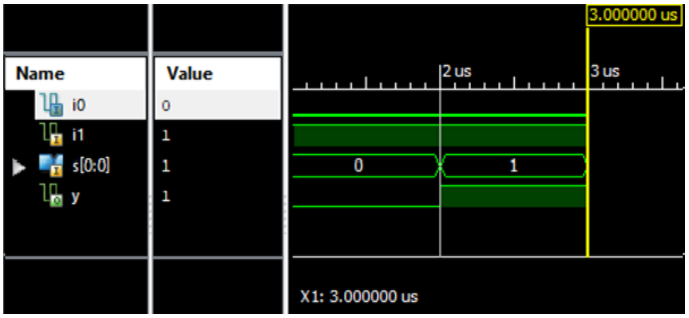


Figure 11. Simulation waveforms of (2×1) Mux

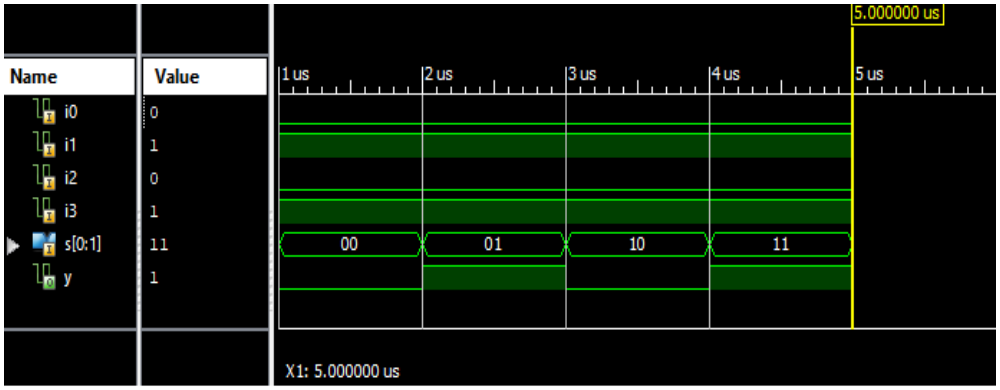


Figure 12. Simulation waveforms of (4×1) Mux

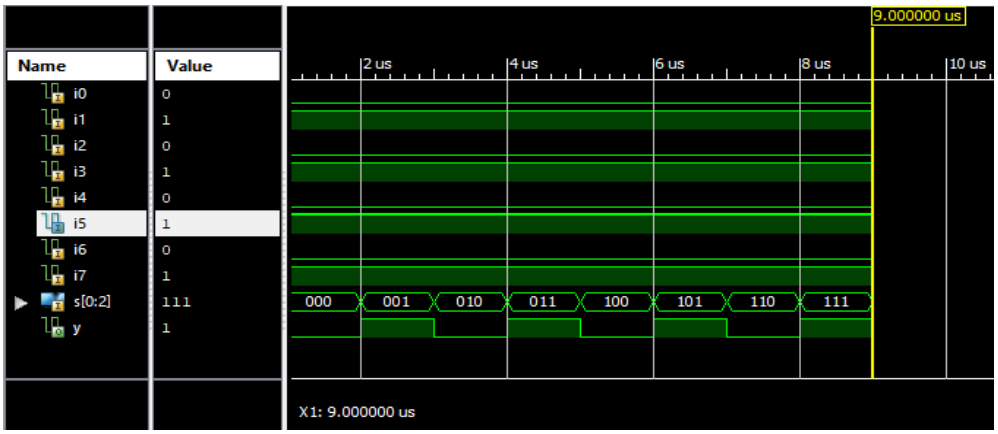


Figure 13. Simulation waveforms of (8×1) Mux

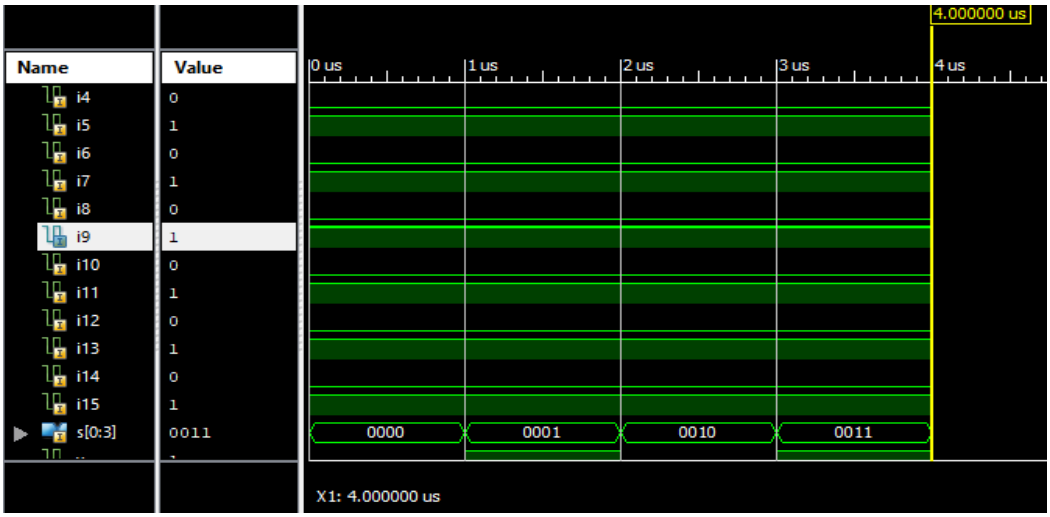


Figure 14. Simulation waveforms of (16×1) Mux

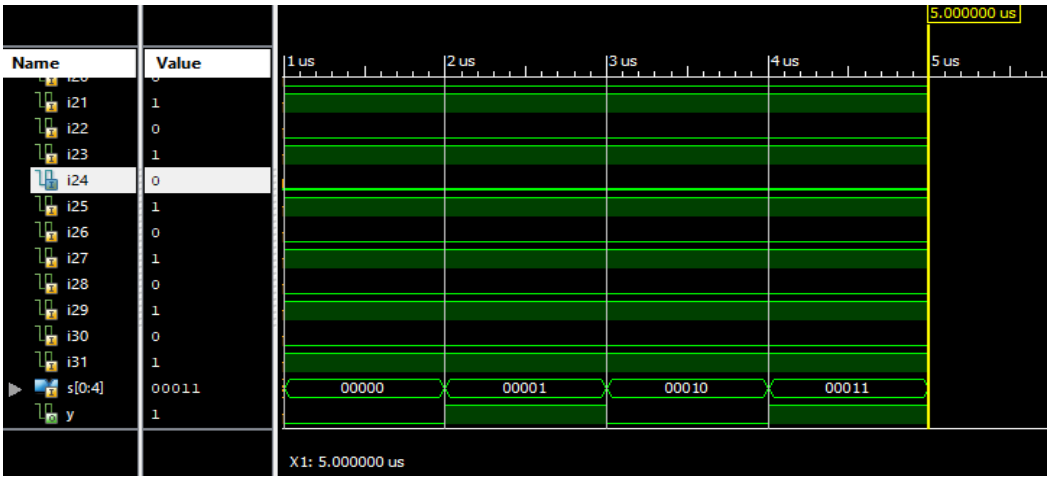


Figure 15. Simulation waveforms of (32×1) Mux

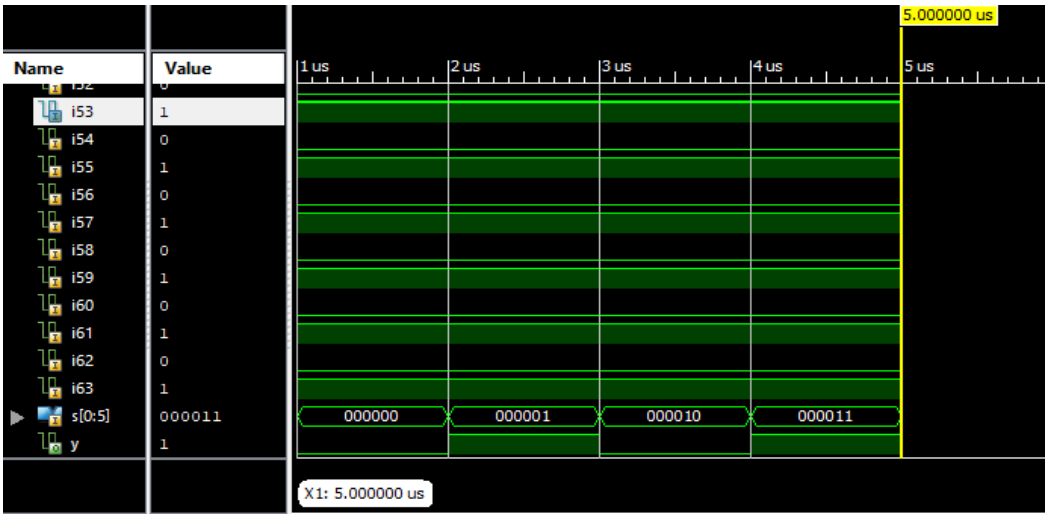


Figure 16. Simulation waveforms of (64×1) Mux

Table 5. Result comparison of multiplexers various configurations on different hardware

Design	Slices	Flip-flops	LUTs	I/Os	Delay (ns)	Memory (KB)	Power (mW)
Mux				Virtex-5			
2×1	1/28800	0/1	1/28800	4/480	3.809	4550292	110.05
4×1	1/28800	0/1	1/28800	7/480	4.110	4549972	121.90
8×1	2/28800	0/2	2/28800	12/480	4.328	4550292	205.10
16×1	5/28800	0/5	5/28800	21/480	4.910	4549908	355.40
32×1	10/28800	0/10	10/28800	38/480	5.261	4550292	405.00
64×1	21/28800	0/21	21/28800	71/480	5.871	4550228	605.20
Mux				SPARTAN-3E			
2×1	1/960	-	1/1920	4/66	5.753	4519956	120.00
4×1	1/960	-	2/1920	7/66	6.054	4520084	12550
8×1	2/960	-	4/1920	12/66	6.624	4520452	212.17
16×1	4/960	-	8/1920	21/66	7.219	4520852	375.90
32×1	8/960	-	16/1920	38/66	7.906	4520916	415.00
64×1	17/960	-	33/1920	71/66	9.138	4520596	625.00
Mux				Virtex-6			
2×1	1/46560	0/1	1/46560	4/240	0.918	4519912	105.00
4×1	1/46560	0/1	1/46560	7/240	0.933	4547240	109.58
8×1	2/46560	0/2	2/46560	12/240	1.124	4547240	195.45
16×1	4/46560	0/4	4/46560	21/240	1.265	4547560	310.25
32×1	4/46560	0/4	4/46560	21/240	1.686	4547560	378.90
64×1	21/46560	0/21	21/46560	71/240	2.440	4547560	550.30
Mux				SPARTAN-6			
2×1	1/27288	0/1	1/27288	4/316	5.385	4523432	115.90
4×1	1/27288	0/1	1/27288	7/316	5.519	4522920	123.50
8×1	2/27288	0/2	2/27288	12/316	5.696	4522920	210.52
16×1	4/27288	0/4	4/27288	21/316	5.914	4523240	362.50
32×1	10/27288	0/10	10/27288	38/316	7.961	4523688	410.50
64×1	21/27288	0/21	21/27288	71/316	8.003	4523560	618.00

5. CONCLUSION

The hardware chip design of the different configuration multiplexer is done successfully on Xilinx ISE14.7. The simulation of the design is carried out successfully on Modelsim 10.0 software. The chip design is considered for the different sizes of the Mux such as (2×1), (4×1), (8×1), (16×1), (32×1), and (64×1). The design is based on the concept of scalable design and a behavioral model is followed to estimate the performance of the system on different FPGA hardware kits such as Virtex-5, Virtex-6, SPARTAN-3E, and SPARTAN-6. The total delay of (64×1) Mux design is 5.871 ns, 2.440 ns, 9.138 ns, and 8.003 ns for Virtex-5, Virtex-6, SPARTAN-3E, and SPARTAN-6 respectively. The memory usage of (64×1) Mux is 4550228 KB, 4547560 KB, 4520596 KB, and 4523560 KB for Virtex-5, Virtex-6, SPARTAN-3E, and SPARTAN-6 respectively. The power consumption is 625.00 mW, 618.00 mW, 605.20 mW, and 550.30 mW for (64×1) Mux for SPARTAN-3E, SPARTAN-6, Virtex-5 and Virtex-6 FPGA respectively. The study concludes that the Virtex-6 provides the optimal hardware, power, and timing performance in comparison to other FPGAs.

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AUTHOR CONTRIBUTIONS STATEMENT

This journal uses the Contributor Roles Taxonomy (CRediT) to recognize individual author contributions, reduce authorship disputes, and facilitate collaboration.

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Adesh Kumar	✓	✓				✓	✓	✓	✓	✓	✓	✓		
Anurag Vijay Agrawal	✓		✓	✓			✓			✓	✓	✓	✓	

C : **C**onceptualization
M : **M**ethodology
So : **So**ftware
Va : **Va**lidation
Fo : **Fo**rmal analysis
I : **I**nvestigation
R : **R**esources
D : **D**ata Curation
O : Writing - **O**riginal Draft
E : Writing - Review & **E**diting
Vi : **Vi**sualization
Su : **Su**pervision
P : **P**roject administration
Fu : **Fu**nding acquisition

CONFLICT OF INTEREST STATEMENT

The authors state no conflict of interest.

DATA AVAILABILITY

The authors confirm that the data supporting the findings of this study are available within the article.

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